---------- Begin Simulation Statistics ----------

sim\_seconds 0.000033 # Number of seconds simulated

sim\_ticks 33361500 # Number of ticks simulated

final\_tick 33361500 # Number of ticks from beginning of simulation (restored from checkpoints and never reset)

sim\_freq 1000000000000 # Frequency of simulated ticks

host\_inst\_rate 127116 # Simulator instruction rate (inst/s)

host\_op\_rate 127077 # Simulator op (including micro ops) rate (op/s)

host\_tick\_rate 819956812 # Simulator tick rate (ticks/s)

host\_mem\_usage 642656 # Number of bytes of host memory used

host\_seconds 0.04 # Real time elapsed on the host

sim\_insts 5169 # Number of instructions simulated

sim\_ops 5169 # Number of ops (including micro ops) simulated

system.voltage\_domain.voltage 1 # Voltage in Volts

system.clk\_domain.clock 1000 # Clock period in ticks

system.mem\_ctrls.pwrStateResidencyTicks::UNDEFINED 33361500 # Cumulative time (in ticks) in various power states

system.mem\_ctrls.bytes\_read::.cpu.inst 25856 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_read::.cpu.data 9280 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_read::total 35136 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_inst\_read::.cpu.inst 25856 # Number of instructions bytes read from this memory

system.mem\_ctrls.bytes\_inst\_read::total 25856 # Number of instructions bytes read from this memory

system.mem\_ctrls.num\_reads::.cpu.inst 404 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_reads::.cpu.data 145 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_reads::total 549 # Number of read requests responded to by this memory

system.mem\_ctrls.bw\_read::.cpu.inst 775025104 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_read::.cpu.data 278164951 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_read::total 1053190054 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_inst\_read::.cpu.inst 775025104 # Instruction read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_inst\_read::total 775025104 # Instruction read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_total::.cpu.inst 775025104 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::.cpu.data 278164951 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::total 1053190054 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.avgPriority\_.writebacks::samples 80.00 # Average QoS priority value for accepted requests

system.mem\_ctrls.avgPriority\_.cpu.inst::samples 404.00 # Average QoS priority value for accepted requests

system.mem\_ctrls.avgPriority\_.cpu.data::samples 145.00 # Average QoS priority value for accepted requests

system.mem\_ctrls.priorityMinLatency 0.000000018750 # per QoS priority minimum request to response latency (s)

system.mem\_ctrls.priorityMaxLatency 0.000038256750 # per QoS priority maximum request to response latency (s)

system.mem\_ctrls.numReadWriteTurnArounds 3 # Number of turnarounds from READ to WRITE

system.mem\_ctrls.numWriteReadTurnArounds 3 # Number of turnarounds from WRITE to READ

system.mem\_ctrls.numStayReadState 1177 # Number of times bus staying in READ state

system.mem\_ctrls.numStayWriteState 45 # Number of times bus staying in WRITE state

system.mem\_ctrls.readReqs 549 # Number of read requests accepted

system.mem\_ctrls.writeReqs 80 # Number of write requests accepted

system.mem\_ctrls.readBursts 549 # Number of DRAM read bursts, including those serviced by the write queue

system.mem\_ctrls.writeBursts 80 # Number of DRAM write bursts, including those merged in the write queue

system.mem\_ctrls.bytesReadDRAM 35136 # Total number of bytes read from DRAM

system.mem\_ctrls.bytesReadWrQ 0 # Total number of bytes read from write queue

system.mem\_ctrls.bytesWritten 3072 # Total number of bytes written to DRAM

system.mem\_ctrls.bytesReadSys 35136 # Total read bytes from the system interface side

system.mem\_ctrls.bytesWrittenSys 5120 # Total written bytes from the system interface side

system.mem\_ctrls.servicedByWrQ 0 # Number of DRAM read bursts serviced by the write queue

system.mem\_ctrls.mergedWrBursts 0 # Number of DRAM write bursts merged with an existing one

system.mem\_ctrls.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write

system.mem\_ctrls.perBankRdBursts::0 84 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::1 46 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::2 61 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::3 52 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::4 39 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::5 80 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::6 104 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::7 20 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::8 3 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::9 28 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::10 0 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::11 0 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::12 21 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::13 9 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::14 1 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::15 1 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::0 13 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::1 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::2 13 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::3 4 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::4 1 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::5 1 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::6 15 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::7 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::8 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::9 1 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::10 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::11 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::12 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::13 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::14 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::15 0 # Per bank write bursts

system.mem\_ctrls.numRdRetry 0 # Number of times read queue was full causing retry

system.mem\_ctrls.numWrRetry 0 # Number of times write queue was full causing retry

system.mem\_ctrls.totGap 33279500 # Total gap between requests

system.mem\_ctrls.readPktSize::0 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::1 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::2 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::3 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::4 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::5 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::6 549 # Read request sizes (log2)

system.mem\_ctrls.writePktSize::0 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::1 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::2 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::3 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::4 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::5 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::6 80 # Write request sizes (log2)

system.mem\_ctrls.rdQLenPdf::0 463 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::1 80 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::2 6 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::3 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::4 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::5 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::6 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::7 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::8 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::9 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::10 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::11 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::12 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::13 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::14 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::15 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::16 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::17 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::18 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::19 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::20 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::21 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::22 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::23 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::24 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::25 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::26 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::27 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::28 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::29 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::30 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::31 0 # What read queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::0 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::1 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::2 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::3 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::4 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::5 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::6 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::7 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::8 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::9 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::10 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::11 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::12 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::13 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::14 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::15 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::16 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::17 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::18 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::19 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::20 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::21 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::22 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::23 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::24 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::25 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::26 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::27 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::28 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::29 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::30 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::31 4 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::32 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::33 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::34 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::35 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::36 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::37 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::38 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::39 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::40 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::41 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::42 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::43 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::44 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::45 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::46 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::47 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::48 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::49 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::50 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::51 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::52 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::53 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::54 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::55 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::56 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::57 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::58 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::59 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::60 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::61 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::62 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::63 0 # What write queue length does an incoming req see

system.mem\_ctrls.bytesPerActivate::samples 98 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::mean 379.428571 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::gmean 240.643490 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::stdev 338.188260 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::0-127 25 25.51% 25.51% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::128-255 21 21.43% 46.94% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::256-383 14 14.29% 61.22% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::384-511 6 6.12% 67.35% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::512-639 7 7.14% 74.49% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::640-767 7 7.14% 81.63% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::768-895 3 3.06% 84.69% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::896-1023 2 2.04% 86.73% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::1024-1151 13 13.27% 100.00% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::total 98 # Bytes accessed per row activation

system.mem\_ctrls.rdPerTurnAround::samples 3 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::mean 170.666667 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::gmean 99.414175 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::stdev 203.266656 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::32-47 1 33.33% 33.33% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::64-79 1 33.33% 66.67% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::400-415 1 33.33% 100.00% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::total 3 # Reads before turning the bus around for writes

system.mem\_ctrls.wrPerTurnAround::samples 3 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::mean 16 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::gmean 16.000000 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::16 3 100.00% 100.00% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::total 3 # Writes before turning the bus around for reads

system.mem\_ctrls.masterReadBytes::.cpu.inst 25856 # Per-master bytes read from memory

system.mem\_ctrls.masterReadBytes::.cpu.data 9280 # Per-master bytes read from memory

system.mem\_ctrls.masterWriteBytes::.writebacks 3072 # Per-master bytes write to memory

system.mem\_ctrls.masterReadRate::.cpu.inst 775025103.787299633026 # Per-master bytes read from memory rate (Bytes/sec)

system.mem\_ctrls.masterReadRate::.cpu.data 278164950.616728842258 # Per-master bytes read from memory rate (Bytes/sec)

system.mem\_ctrls.masterWriteRate::.writebacks 92082190.548986107111 # Per-master bytes write to memory rate (Bytes/sec)

system.mem\_ctrls.masterReadAccesses::.cpu.inst 404 # Per-master read serviced memory accesses

system.mem\_ctrls.masterReadAccesses::.cpu.data 145 # Per-master read serviced memory accesses

system.mem\_ctrls.masterWriteAccesses::.writebacks 80 # Per-master write serviced memory accesses

system.mem\_ctrls.masterReadTotalLat::.cpu.inst 12682500 # Per-master read total memory access latency

system.mem\_ctrls.masterReadTotalLat::.cpu.data 4691000 # Per-master read total memory access latency

system.mem\_ctrls.masterWriteTotalLat::.writebacks 340668500 # Per-master write total memory access latency

system.mem\_ctrls.masterReadAvgLat::.cpu.inst 31392.33 # Per-master read average memory access latency

system.mem\_ctrls.masterReadAvgLat::.cpu.data 32351.72 # Per-master read average memory access latency

system.mem\_ctrls.masterWriteAvgLat::.writebacks 4258356.25 # Per-master write average memory access latency

system.mem\_ctrls.totQLat 7079750 # Total ticks spent queuing

system.mem\_ctrls.totMemAccLat 17373500 # Total ticks spent from burst creation until serviced by the DRAM

system.mem\_ctrls.totBusLat 2745000 # Total ticks spent in databus transfers

system.mem\_ctrls.avgQLat 12895.72 # Average queueing delay per DRAM burst

system.mem\_ctrls.avgBusLat 5000.00 # Average bus latency per DRAM burst

system.mem\_ctrls.avgMemAccLat 31645.72 # Average memory access latency per DRAM burst

system.mem\_ctrls.avgRdBW 1053.19 # Average DRAM read bandwidth in MiByte/s

system.mem\_ctrls.avgWrBW 92.08 # Average achieved write bandwidth in MiByte/s

system.mem\_ctrls.avgRdBWSys 1053.19 # Average system read bandwidth in MiByte/s

system.mem\_ctrls.avgWrBWSys 153.47 # Average system write bandwidth in MiByte/s

system.mem\_ctrls.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s

system.mem\_ctrls.busUtil 8.95 # Data bus utilization in percentage

system.mem\_ctrls.busUtilRead 8.23 # Data bus utilization in percentage for reads

system.mem\_ctrls.busUtilWrite 0.72 # Data bus utilization in percentage for writes

system.mem\_ctrls.avgRdQLen 1.18 # Average read queue length when enqueuing

system.mem\_ctrls.avgWrQLen 13.59 # Average write queue length when enqueuing

system.mem\_ctrls.readRowHits 454 # Number of row buffer hits during reads

system.mem\_ctrls.writeRowHits 42 # Number of row buffer hits during writes

system.mem\_ctrls.readRowHitRate 82.70 # Row buffer hit rate for reads

system.mem\_ctrls.writeRowHitRate 52.50 # Row buffer hit rate for writes

system.mem\_ctrls.avgGap 52908.59 # Average gap between requests

system.mem\_ctrls.pageHitRate 78.86 # Row buffer hit rate, read and write combined

system.mem\_ctrls\_0.actEnergy 621180 # Energy for activate commands per rank (pJ)

system.mem\_ctrls\_0.preEnergy 318780 # Energy for precharge commands per rank (pJ)

system.mem\_ctrls\_0.readEnergy 3470040 # Energy for read commands per rank (pJ)

system.mem\_ctrls\_0.writeEnergy 245340 # Energy for write commands per rank (pJ)

system.mem\_ctrls\_0.refreshEnergy 2458560.000000 # Energy for refresh commands per rank (pJ)

system.mem\_ctrls\_0.actBackEnergy 6740250 # Energy for active background per rank (pJ)

system.mem\_ctrls\_0.preBackEnergy 51360 # Energy for precharge background per rank (pJ)

system.mem\_ctrls\_0.actPowerDownEnergy 8410350 # Energy for active power-down per rank (pJ)

system.mem\_ctrls\_0.prePowerDownEnergy 1440 # Energy for precharge power-down per rank (pJ)

system.mem\_ctrls\_0.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ)

system.mem\_ctrls\_0.totalEnergy 22317300 # Total energy per rank (pJ)

system.mem\_ctrls\_0.averagePower 668.953734 # Core power per rank (mW)

system.mem\_ctrls\_0.totalIdleTime 18406250 # Total Idle time Per DRAM Rank

system.mem\_ctrls\_0.memoryStateTime::IDLE 23000 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::REF 1040000 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::SREF 0 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::PRE\_PDN 3750 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::ACT 13853750 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::ACT\_PDN 18441000 # Time in different power states

system.mem\_ctrls\_1.actEnergy 99960 # Energy for activate commands per rank (pJ)

system.mem\_ctrls\_1.preEnergy 53130 # Energy for precharge commands per rank (pJ)

system.mem\_ctrls\_1.readEnergy 449820 # Energy for read commands per rank (pJ)

system.mem\_ctrls\_1.writeEnergy 5220 # Energy for write commands per rank (pJ)

system.mem\_ctrls\_1.refreshEnergy 2458560.000000 # Energy for refresh commands per rank (pJ)

system.mem\_ctrls\_1.actBackEnergy 1429560 # Energy for active background per rank (pJ)

system.mem\_ctrls\_1.preBackEnergy 228960 # Energy for precharge background per rank (pJ)

system.mem\_ctrls\_1.actPowerDownEnergy 11076240 # Energy for active power-down per rank (pJ)

system.mem\_ctrls\_1.prePowerDownEnergy 2051040 # Energy for precharge power-down per rank (pJ)

system.mem\_ctrls\_1.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ)

system.mem\_ctrls\_1.totalEnergy 17852490 # Total energy per rank (pJ)

system.mem\_ctrls\_1.averagePower 535.122521 # Core power per rank (mW)

system.mem\_ctrls\_1.totalIdleTime 27693750 # Total Idle time Per DRAM Rank

system.mem\_ctrls\_1.memoryStateTime::IDLE 473000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::REF 1040000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::SREF 0 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::PRE\_PDN 5339000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::ACT 2218000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::ACT\_PDN 24291500 # Time in different power states

system.pwrStateResidencyTicks::UNDEFINED 33361500 # Cumulative time (in ticks) in various power states

system.cpu.branchPred.lookups 1783 # Number of BP lookups

system.cpu.branchPred.condPredicted 1116 # Number of conditional branches predicted

system.cpu.branchPred.condIncorrect 365 # Number of conditional branches incorrect

system.cpu.branchPred.BTBLookups 1458 # Number of BTB lookups

system.cpu.branchPred.BTBHits 311 # Number of BTB hits

system.cpu.branchPred.BTBCorrect 0 # Number of correct BTB predictions (this stat may not work properly.

system.cpu.branchPred.BTBHitPct 21.330590 # BTB Hit Percentage

system.cpu.branchPred.usedRAS 179 # Number of times the RAS was used to get a target.

system.cpu.branchPred.RASInCorrect 14 # Number of incorrect RAS predictions.

system.cpu.branchPred.indirectLookups 93 # Number of indirect predictor lookups.

system.cpu.branchPred.indirectHits 8 # Number of indirect target hits.

system.cpu.branchPred.indirectMisses 85 # Number of indirect misses.

system.cpu.branchPredindirectMispredicted 36 # Number of mispredicted indirect branches.

system.cpu\_voltage\_domain.voltage 1 # Voltage in Volts

system.cpu\_clk\_domain.clock 500 # Clock period in ticks

system.cpu.dtb.fetch\_hits 0 # ITB hits

system.cpu.dtb.fetch\_misses 0 # ITB misses

system.cpu.dtb.fetch\_acv 0 # ITB acv

system.cpu.dtb.fetch\_accesses 0 # ITB accesses

system.cpu.dtb.read\_hits 1096 # DTB read hits

system.cpu.dtb.read\_misses 15 # DTB read misses

system.cpu.dtb.read\_acv 0 # DTB read access violations

system.cpu.dtb.read\_accesses 1111 # DTB read accesses

system.cpu.dtb.write\_hits 885 # DTB write hits

system.cpu.dtb.write\_misses 6 # DTB write misses

system.cpu.dtb.write\_acv 0 # DTB write access violations

system.cpu.dtb.write\_accesses 891 # DTB write accesses

system.cpu.dtb.data\_hits 1981 # DTB hits

system.cpu.dtb.data\_misses 21 # DTB misses

system.cpu.dtb.data\_acv 0 # DTB access violations

system.cpu.dtb.data\_accesses 2002 # DTB accesses

system.cpu.itb.fetch\_hits 2280 # ITB hits

system.cpu.itb.fetch\_misses 18 # ITB misses

system.cpu.itb.fetch\_acv 0 # ITB acv

system.cpu.itb.fetch\_accesses 2298 # ITB accesses

system.cpu.itb.read\_hits 0 # DTB read hits

system.cpu.itb.read\_misses 0 # DTB read misses

system.cpu.itb.read\_acv 0 # DTB read access violations

system.cpu.itb.read\_accesses 0 # DTB read accesses

system.cpu.itb.write\_hits 0 # DTB write hits

system.cpu.itb.write\_misses 0 # DTB write misses

system.cpu.itb.write\_acv 0 # DTB write access violations

system.cpu.itb.write\_accesses 0 # DTB write accesses

system.cpu.itb.data\_hits 0 # DTB hits

system.cpu.itb.data\_misses 0 # DTB misses

system.cpu.itb.data\_acv 0 # DTB access violations

system.cpu.itb.data\_accesses 0 # DTB accesses

system.cpu.workload.numSyscalls 11 # Number of system calls

system.cpu.pwrStateResidencyTicks::ON 33361500 # Cumulative time (in ticks) in various power states

system.cpu.numCycles 66723 # number of cpu cycles simulated

system.cpu.numWorkItemsStarted 0 # number of work items this cpu started

system.cpu.numWorkItemsCompleted 0 # number of work items this cpu completed

system.cpu.committedInsts 5169 # Number of instructions committed

system.cpu.committedOps 5169 # Number of ops (including micro ops) committed

system.cpu.discardedOps 1225 # Number of ops (including micro ops) which were discarded before commit

system.cpu.numFetchSuspends 0 # Number of times Execute suspended instruction fetching

system.cpu.cpi 12.908299 # CPI: cycles per instruction

system.cpu.ipc 0.077470 # IPC: instructions per cycle

system.cpu.op\_class\_0::No\_OpClass 206 3.99% 3.99% # Class of committed instruction

system.cpu.op\_class\_0::IntAlu 3110 60.17% 64.15% # Class of committed instruction

system.cpu.op\_class\_0::IntMult 3 0.06% 64.21% # Class of committed instruction

system.cpu.op\_class\_0::IntDiv 0 0.00% 64.21% # Class of committed instruction

system.cpu.op\_class\_0::FloatAdd 12 0.23% 64.44% # Class of committed instruction

system.cpu.op\_class\_0::FloatCmp 0 0.00% 64.44% # Class of committed instruction

system.cpu.op\_class\_0::FloatCvt 8 0.15% 64.60% # Class of committed instruction

system.cpu.op\_class\_0::FloatMult 0 0.00% 64.60% # Class of committed instruction

system.cpu.op\_class\_0::FloatMultAcc 0 0.00% 64.60% # Class of committed instruction

system.cpu.op\_class\_0::FloatDiv 2 0.04% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::FloatMisc 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::FloatSqrt 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdAdd 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdAddAcc 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdAlu 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdCmp 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdCvt 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdMisc 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdMult 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdMultAcc 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdShift 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdShiftAcc 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdSqrt 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatAdd 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatAlu 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatCmp 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatCvt 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatDiv 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatMisc 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatMult 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatMultAcc 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatSqrt 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdAes 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdAesMix 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdSha1Hash 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdSha1Hash2 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdSha256Hash 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdSha256Hash2 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdShaSigma2 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::SimdShaSigma3 0 0.00% 64.64% # Class of committed instruction

system.cpu.op\_class\_0::MemRead 943 18.24% 82.88% # Class of committed instruction

system.cpu.op\_class\_0::MemWrite 862 16.68% 99.56% # Class of committed instruction

system.cpu.op\_class\_0::FloatMemRead 6 0.12% 99.67% # Class of committed instruction

system.cpu.op\_class\_0::FloatMemWrite 17 0.33% 100.00% # Class of committed instruction

system.cpu.op\_class\_0::IprAccess 0 0.00% 100.00% # Class of committed instruction

system.cpu.op\_class\_0::InstPrefetch 0 0.00% 100.00% # Class of committed instruction

system.cpu.op\_class\_0::total 5169 # Class of committed instruction

system.cpu.tickCycles 11203 # Number of cycles that the object actually ticked

system.cpu.idleCycles 55520 # Total number of cycles that the object has spent stopped

system.cpu.fetch2.int\_instructions 5744 # Number of integer instructions successfully decoded

system.cpu.fetch2.fp\_instructions 45 # Number of floating point instructions successfully decoded

system.cpu.fetch2.vec\_instructions 0 # Number of SIMD instructions successfully decoded

system.cpu.fetch2.load\_instructions 1796 # Number of memory load instructions successfully decoded

system.cpu.fetch2.store\_instructions 1306 # Number of memory store instructions successfully decoded

system.cpu.dcache.tags.pwrStateResidencyTicks::UNDEFINED 33361500 # Cumulative time (in ticks) in various power states

system.cpu.dcache.tags.tagsinuse 95.143670 # Cycle average of tags in use

system.cpu.dcache.tags.total\_refs 1892 # Total number of references to valid blocks.

system.cpu.dcache.tags.sampled\_refs 145 # Sample count of references to valid blocks.

system.cpu.dcache.tags.avg\_refs 13.048276 # Average number of references to valid blocks.

system.cpu.dcache.tags.warmup\_cycle 210000 # Cycle when the warmup percentage was hit.

system.cpu.dcache.tags.occ\_blocks::.cpu.data 95.143670 # Average occupied blocks per requestor

system.cpu.dcache.tags.occ\_percent::.cpu.data 0.092914 # Average percentage of cache occupancy

system.cpu.dcache.tags.occ\_percent::total 0.092914 # Average percentage of cache occupancy

system.cpu.dcache.tags.occ\_task\_id\_blocks::1024 145 # Occupied blocks per task id

system.cpu.dcache.tags.age\_task\_id\_blocks\_1024::0 14 # Occupied blocks per task id

system.cpu.dcache.tags.age\_task\_id\_blocks\_1024::1 131 # Occupied blocks per task id

system.cpu.dcache.tags.occ\_task\_id\_percent::1024 0.141602 # Percentage of cache occupancy per task id

system.cpu.dcache.tags.tag\_accesses 4043 # Number of tag accesses

system.cpu.dcache.tags.data\_accesses 4043 # Number of data accesses

system.cpu.dcache.pwrStateResidencyTicks::UNDEFINED 33361500 # Cumulative time (in ticks) in various power states

system.cpu.dcache.ReadReq\_hits::.cpu.data 991 # number of ReadReq hits

system.cpu.dcache.ReadReq\_hits::total 991 # number of ReadReq hits

system.cpu.dcache.WriteReq\_hits::.cpu.data 732 # number of WriteReq hits

system.cpu.dcache.WriteReq\_hits::total 732 # number of WriteReq hits

system.cpu.dcache.LoadLockedReq\_hits::.cpu.data 12 # number of LoadLockedReq hits

system.cpu.dcache.LoadLockedReq\_hits::total 12 # number of LoadLockedReq hits

system.cpu.dcache.StoreCondReq\_hits::.cpu.data 12 # number of StoreCondReq hits

system.cpu.dcache.StoreCondReq\_hits::total 12 # number of StoreCondReq hits

system.cpu.dcache.demand\_hits::.cpu.data 1723 # number of demand (read+write) hits

system.cpu.dcache.demand\_hits::total 1723 # number of demand (read+write) hits

system.cpu.dcache.overall\_hits::.cpu.data 1723 # number of overall hits

system.cpu.dcache.overall\_hits::total 1723 # number of overall hits

system.cpu.dcache.ReadReq\_misses::.cpu.data 73 # number of ReadReq misses

system.cpu.dcache.ReadReq\_misses::total 73 # number of ReadReq misses

system.cpu.dcache.WriteReq\_misses::.cpu.data 129 # number of WriteReq misses

system.cpu.dcache.WriteReq\_misses::total 129 # number of WriteReq misses

system.cpu.dcache.demand\_misses::.cpu.data 202 # number of demand (read+write) misses

system.cpu.dcache.demand\_misses::total 202 # number of demand (read+write) misses

system.cpu.dcache.overall\_misses::.cpu.data 202 # number of overall misses

system.cpu.dcache.overall\_misses::total 202 # number of overall misses

system.cpu.dcache.ReadReq\_miss\_latency::.cpu.data 4973500 # number of ReadReq miss cycles

system.cpu.dcache.ReadReq\_miss\_latency::total 4973500 # number of ReadReq miss cycles

system.cpu.dcache.WriteReq\_miss\_latency::.cpu.data 7945500 # number of WriteReq miss cycles

system.cpu.dcache.WriteReq\_miss\_latency::total 7945500 # number of WriteReq miss cycles

system.cpu.dcache.demand\_miss\_latency::.cpu.data 12919000 # number of demand (read+write) miss cycles

system.cpu.dcache.demand\_miss\_latency::total 12919000 # number of demand (read+write) miss cycles

system.cpu.dcache.overall\_miss\_latency::.cpu.data 12919000 # number of overall miss cycles

system.cpu.dcache.overall\_miss\_latency::total 12919000 # number of overall miss cycles

system.cpu.dcache.ReadReq\_accesses::.cpu.data 1064 # number of ReadReq accesses(hits+misses)

system.cpu.dcache.ReadReq\_accesses::total 1064 # number of ReadReq accesses(hits+misses)

system.cpu.dcache.WriteReq\_accesses::.cpu.data 861 # number of WriteReq accesses(hits+misses)

system.cpu.dcache.WriteReq\_accesses::total 861 # number of WriteReq accesses(hits+misses)

system.cpu.dcache.LoadLockedReq\_accesses::.cpu.data 12 # number of LoadLockedReq accesses(hits+misses)

system.cpu.dcache.LoadLockedReq\_accesses::total 12 # number of LoadLockedReq accesses(hits+misses)

system.cpu.dcache.StoreCondReq\_accesses::.cpu.data 12 # number of StoreCondReq accesses(hits+misses)

system.cpu.dcache.StoreCondReq\_accesses::total 12 # number of StoreCondReq accesses(hits+misses)

system.cpu.dcache.demand\_accesses::.cpu.data 1925 # number of demand (read+write) accesses

system.cpu.dcache.demand\_accesses::total 1925 # number of demand (read+write) accesses

system.cpu.dcache.overall\_accesses::.cpu.data 1925 # number of overall (read+write) accesses

system.cpu.dcache.overall\_accesses::total 1925 # number of overall (read+write) accesses

system.cpu.dcache.ReadReq\_miss\_rate::.cpu.data 0.068609 # miss rate for ReadReq accesses

system.cpu.dcache.ReadReq\_miss\_rate::total 0.068609 # miss rate for ReadReq accesses

system.cpu.dcache.WriteReq\_miss\_rate::.cpu.data 0.149826 # miss rate for WriteReq accesses

system.cpu.dcache.WriteReq\_miss\_rate::total 0.149826 # miss rate for WriteReq accesses

system.cpu.dcache.demand\_miss\_rate::.cpu.data 0.104935 # miss rate for demand accesses

system.cpu.dcache.demand\_miss\_rate::total 0.104935 # miss rate for demand accesses

system.cpu.dcache.overall\_miss\_rate::.cpu.data 0.104935 # miss rate for overall accesses

system.cpu.dcache.overall\_miss\_rate::total 0.104935 # miss rate for overall accesses

system.cpu.dcache.ReadReq\_avg\_miss\_latency::.cpu.data 68130.136986 # average ReadReq miss latency

system.cpu.dcache.ReadReq\_avg\_miss\_latency::total 68130.136986 # average ReadReq miss latency

system.cpu.dcache.WriteReq\_avg\_miss\_latency::.cpu.data 61593.023256 # average WriteReq miss latency

system.cpu.dcache.WriteReq\_avg\_miss\_latency::total 61593.023256 # average WriteReq miss latency

system.cpu.dcache.demand\_avg\_miss\_latency::.cpu.data 63955.445545 # average overall miss latency

system.cpu.dcache.demand\_avg\_miss\_latency::total 63955.445545 # average overall miss latency

system.cpu.dcache.overall\_avg\_miss\_latency::.cpu.data 63955.445545 # average overall miss latency

system.cpu.dcache.overall\_avg\_miss\_latency::total 63955.445545 # average overall miss latency

system.cpu.dcache.blocked\_cycles::no\_mshrs 0 # number of cycles access was blocked

system.cpu.dcache.blocked\_cycles::no\_targets 0 # number of cycles access was blocked

system.cpu.dcache.blocked::no\_mshrs 0 # number of cycles access was blocked

system.cpu.dcache.blocked::no\_targets 0 # number of cycles access was blocked

system.cpu.dcache.avg\_blocked\_cycles::no\_mshrs nan # average number of cycles each access was blocked

system.cpu.dcache.avg\_blocked\_cycles::no\_targets nan # average number of cycles each access was blocked

system.cpu.dcache.ReadReq\_mshr\_hits::.cpu.data 3 # number of ReadReq MSHR hits

system.cpu.dcache.ReadReq\_mshr\_hits::total 3 # number of ReadReq MSHR hits

system.cpu.dcache.WriteReq\_mshr\_hits::.cpu.data 54 # number of WriteReq MSHR hits

system.cpu.dcache.WriteReq\_mshr\_hits::total 54 # number of WriteReq MSHR hits

system.cpu.dcache.demand\_mshr\_hits::.cpu.data 57 # number of demand (read+write) MSHR hits

system.cpu.dcache.demand\_mshr\_hits::total 57 # number of demand (read+write) MSHR hits

system.cpu.dcache.overall\_mshr\_hits::.cpu.data 57 # number of overall MSHR hits

system.cpu.dcache.overall\_mshr\_hits::total 57 # number of overall MSHR hits

system.cpu.dcache.ReadReq\_mshr\_misses::.cpu.data 70 # number of ReadReq MSHR misses

system.cpu.dcache.ReadReq\_mshr\_misses::total 70 # number of ReadReq MSHR misses

system.cpu.dcache.WriteReq\_mshr\_misses::.cpu.data 75 # number of WriteReq MSHR misses

system.cpu.dcache.WriteReq\_mshr\_misses::total 75 # number of WriteReq MSHR misses

system.cpu.dcache.demand\_mshr\_misses::.cpu.data 145 # number of demand (read+write) MSHR misses

system.cpu.dcache.demand\_mshr\_misses::total 145 # number of demand (read+write) MSHR misses

system.cpu.dcache.overall\_mshr\_misses::.cpu.data 145 # number of overall MSHR misses

system.cpu.dcache.overall\_mshr\_misses::total 145 # number of overall MSHR misses

system.cpu.dcache.ReadReq\_mshr\_miss\_latency::.cpu.data 4717000 # number of ReadReq MSHR miss cycles

system.cpu.dcache.ReadReq\_mshr\_miss\_latency::total 4717000 # number of ReadReq MSHR miss cycles

system.cpu.dcache.WriteReq\_mshr\_miss\_latency::.cpu.data 4594000 # number of WriteReq MSHR miss cycles

system.cpu.dcache.WriteReq\_mshr\_miss\_latency::total 4594000 # number of WriteReq MSHR miss cycles

system.cpu.dcache.demand\_mshr\_miss\_latency::.cpu.data 9311000 # number of demand (read+write) MSHR miss cycles

system.cpu.dcache.demand\_mshr\_miss\_latency::total 9311000 # number of demand (read+write) MSHR miss cycles

system.cpu.dcache.overall\_mshr\_miss\_latency::.cpu.data 9311000 # number of overall MSHR miss cycles

system.cpu.dcache.overall\_mshr\_miss\_latency::total 9311000 # number of overall MSHR miss cycles

system.cpu.dcache.ReadReq\_mshr\_miss\_rate::.cpu.data 0.065789 # mshr miss rate for ReadReq accesses

system.cpu.dcache.ReadReq\_mshr\_miss\_rate::total 0.065789 # mshr miss rate for ReadReq accesses

system.cpu.dcache.WriteReq\_mshr\_miss\_rate::.cpu.data 0.087108 # mshr miss rate for WriteReq accesses

system.cpu.dcache.WriteReq\_mshr\_miss\_rate::total 0.087108 # mshr miss rate for WriteReq accesses

system.cpu.dcache.demand\_mshr\_miss\_rate::.cpu.data 0.075325 # mshr miss rate for demand accesses

system.cpu.dcache.demand\_mshr\_miss\_rate::total 0.075325 # mshr miss rate for demand accesses

system.cpu.dcache.overall\_mshr\_miss\_rate::.cpu.data 0.075325 # mshr miss rate for overall accesses

system.cpu.dcache.overall\_mshr\_miss\_rate::total 0.075325 # mshr miss rate for overall accesses

system.cpu.dcache.ReadReq\_avg\_mshr\_miss\_latency::.cpu.data 67385.714286 # average ReadReq mshr miss latency

system.cpu.dcache.ReadReq\_avg\_mshr\_miss\_latency::total 67385.714286 # average ReadReq mshr miss latency

system.cpu.dcache.WriteReq\_avg\_mshr\_miss\_latency::.cpu.data 61253.333333 # average WriteReq mshr miss latency

system.cpu.dcache.WriteReq\_avg\_mshr\_miss\_latency::total 61253.333333 # average WriteReq mshr miss latency

system.cpu.dcache.demand\_avg\_mshr\_miss\_latency::.cpu.data 64213.793103 # average overall mshr miss latency

system.cpu.dcache.demand\_avg\_mshr\_miss\_latency::total 64213.793103 # average overall mshr miss latency

system.cpu.dcache.overall\_avg\_mshr\_miss\_latency::.cpu.data 64213.793103 # average overall mshr miss latency

system.cpu.dcache.overall\_avg\_mshr\_miss\_latency::total 64213.793103 # average overall mshr miss latency

system.cpu.dcache.replacements 0 # number of replacements

system.cpu.icache.tags.pwrStateResidencyTicks::UNDEFINED 33361500 # Cumulative time (in ticks) in various power states

system.cpu.icache.tags.tagsinuse 176.755216 # Cycle average of tags in use

system.cpu.icache.tags.total\_refs 2280 # Total number of references to valid blocks.

system.cpu.icache.tags.sampled\_refs 404 # Sample count of references to valid blocks.

system.cpu.icache.tags.avg\_refs 5.643564 # Average number of references to valid blocks.

system.cpu.icache.tags.warmup\_cycle 77000 # Cycle when the warmup percentage was hit.

system.cpu.icache.tags.occ\_blocks::.cpu.inst 176.755216 # Average occupied blocks per requestor

system.cpu.icache.tags.occ\_percent::.cpu.inst 0.345225 # Average percentage of cache occupancy

system.cpu.icache.tags.occ\_percent::total 0.345225 # Average percentage of cache occupancy

system.cpu.icache.tags.occ\_task\_id\_blocks::1024 324 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::0 124 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::1 200 # Occupied blocks per task id

system.cpu.icache.tags.occ\_task\_id\_percent::1024 0.632812 # Percentage of cache occupancy per task id

system.cpu.icache.tags.tag\_accesses 4964 # Number of tag accesses

system.cpu.icache.tags.data\_accesses 4964 # Number of data accesses

system.cpu.icache.pwrStateResidencyTicks::UNDEFINED 33361500 # Cumulative time (in ticks) in various power states

system.cpu.icache.ReadReq\_hits::.cpu.inst 1876 # number of ReadReq hits

system.cpu.icache.ReadReq\_hits::total 1876 # number of ReadReq hits

system.cpu.icache.demand\_hits::.cpu.inst 1876 # number of demand (read+write) hits

system.cpu.icache.demand\_hits::total 1876 # number of demand (read+write) hits

system.cpu.icache.overall\_hits::.cpu.inst 1876 # number of overall hits

system.cpu.icache.overall\_hits::total 1876 # number of overall hits

system.cpu.icache.ReadReq\_misses::.cpu.inst 404 # number of ReadReq misses

system.cpu.icache.ReadReq\_misses::total 404 # number of ReadReq misses

system.cpu.icache.demand\_misses::.cpu.inst 404 # number of demand (read+write) misses

system.cpu.icache.demand\_misses::total 404 # number of demand (read+write) misses

system.cpu.icache.overall\_misses::.cpu.inst 404 # number of overall misses

system.cpu.icache.overall\_misses::total 404 # number of overall misses

system.cpu.icache.ReadReq\_miss\_latency::.cpu.inst 25925500 # number of ReadReq miss cycles

system.cpu.icache.ReadReq\_miss\_latency::total 25925500 # number of ReadReq miss cycles

system.cpu.icache.demand\_miss\_latency::.cpu.inst 25925500 # number of demand (read+write) miss cycles

system.cpu.icache.demand\_miss\_latency::total 25925500 # number of demand (read+write) miss cycles

system.cpu.icache.overall\_miss\_latency::.cpu.inst 25925500 # number of overall miss cycles

system.cpu.icache.overall\_miss\_latency::total 25925500 # number of overall miss cycles

system.cpu.icache.ReadReq\_accesses::.cpu.inst 2280 # number of ReadReq accesses(hits+misses)

system.cpu.icache.ReadReq\_accesses::total 2280 # number of ReadReq accesses(hits+misses)

system.cpu.icache.demand\_accesses::.cpu.inst 2280 # number of demand (read+write) accesses

system.cpu.icache.demand\_accesses::total 2280 # number of demand (read+write) accesses

system.cpu.icache.overall\_accesses::.cpu.inst 2280 # number of overall (read+write) accesses

system.cpu.icache.overall\_accesses::total 2280 # number of overall (read+write) accesses

system.cpu.icache.ReadReq\_miss\_rate::.cpu.inst 0.177193 # miss rate for ReadReq accesses

system.cpu.icache.ReadReq\_miss\_rate::total 0.177193 # miss rate for ReadReq accesses

system.cpu.icache.demand\_miss\_rate::.cpu.inst 0.177193 # miss rate for demand accesses

system.cpu.icache.demand\_miss\_rate::total 0.177193 # miss rate for demand accesses

system.cpu.icache.overall\_miss\_rate::.cpu.inst 0.177193 # miss rate for overall accesses

system.cpu.icache.overall\_miss\_rate::total 0.177193 # miss rate for overall accesses

system.cpu.icache.ReadReq\_avg\_miss\_latency::.cpu.inst 64172.029703 # average ReadReq miss latency

system.cpu.icache.ReadReq\_avg\_miss\_latency::total 64172.029703 # average ReadReq miss latency

system.cpu.icache.demand\_avg\_miss\_latency::.cpu.inst 64172.029703 # average overall miss latency

system.cpu.icache.demand\_avg\_miss\_latency::total 64172.029703 # average overall miss latency

system.cpu.icache.overall\_avg\_miss\_latency::.cpu.inst 64172.029703 # average overall miss latency

system.cpu.icache.overall\_avg\_miss\_latency::total 64172.029703 # average overall miss latency

system.cpu.icache.blocked\_cycles::no\_mshrs 0 # number of cycles access was blocked

system.cpu.icache.blocked\_cycles::no\_targets 0 # number of cycles access was blocked

system.cpu.icache.blocked::no\_mshrs 0 # number of cycles access was blocked

system.cpu.icache.blocked::no\_targets 0 # number of cycles access was blocked

system.cpu.icache.avg\_blocked\_cycles::no\_mshrs nan # average number of cycles each access was blocked

system.cpu.icache.avg\_blocked\_cycles::no\_targets nan # average number of cycles each access was blocked

system.cpu.icache.writebacks::.writebacks 80 # number of writebacks

system.cpu.icache.writebacks::total 80 # number of writebacks

system.cpu.icache.ReadReq\_mshr\_misses::.cpu.inst 404 # number of ReadReq MSHR misses

system.cpu.icache.ReadReq\_mshr\_misses::total 404 # number of ReadReq MSHR misses

system.cpu.icache.demand\_mshr\_misses::.cpu.inst 404 # number of demand (read+write) MSHR misses

system.cpu.icache.demand\_mshr\_misses::total 404 # number of demand (read+write) MSHR misses

system.cpu.icache.overall\_mshr\_misses::.cpu.inst 404 # number of overall MSHR misses

system.cpu.icache.overall\_mshr\_misses::total 404 # number of overall MSHR misses

system.cpu.icache.ReadReq\_mshr\_miss\_latency::.cpu.inst 25521500 # number of ReadReq MSHR miss cycles

system.cpu.icache.ReadReq\_mshr\_miss\_latency::total 25521500 # number of ReadReq MSHR miss cycles

system.cpu.icache.demand\_mshr\_miss\_latency::.cpu.inst 25521500 # number of demand (read+write) MSHR miss cycles

system.cpu.icache.demand\_mshr\_miss\_latency::total 25521500 # number of demand (read+write) MSHR miss cycles

system.cpu.icache.overall\_mshr\_miss\_latency::.cpu.inst 25521500 # number of overall MSHR miss cycles

system.cpu.icache.overall\_mshr\_miss\_latency::total 25521500 # number of overall MSHR miss cycles

system.cpu.icache.ReadReq\_mshr\_miss\_rate::.cpu.inst 0.177193 # mshr miss rate for ReadReq accesses

system.cpu.icache.ReadReq\_mshr\_miss\_rate::total 0.177193 # mshr miss rate for ReadReq accesses

system.cpu.icache.demand\_mshr\_miss\_rate::.cpu.inst 0.177193 # mshr miss rate for demand accesses

system.cpu.icache.demand\_mshr\_miss\_rate::total 0.177193 # mshr miss rate for demand accesses

system.cpu.icache.overall\_mshr\_miss\_rate::.cpu.inst 0.177193 # mshr miss rate for overall accesses

system.cpu.icache.overall\_mshr\_miss\_rate::total 0.177193 # mshr miss rate for overall accesses

system.cpu.icache.ReadReq\_avg\_mshr\_miss\_latency::.cpu.inst 63172.029703 # average ReadReq mshr miss latency

system.cpu.icache.ReadReq\_avg\_mshr\_miss\_latency::total 63172.029703 # average ReadReq mshr miss latency

system.cpu.icache.demand\_avg\_mshr\_miss\_latency::.cpu.inst 63172.029703 # average overall mshr miss latency

system.cpu.icache.demand\_avg\_mshr\_miss\_latency::total 63172.029703 # average overall mshr miss latency

system.cpu.icache.overall\_avg\_mshr\_miss\_latency::.cpu.inst 63172.029703 # average overall mshr miss latency

system.cpu.icache.overall\_avg\_mshr\_miss\_latency::total 63172.029703 # average overall mshr miss latency

system.cpu.icache.replacements 80 # number of replacements

system.membus.snoop\_filter.tot\_requests 629 # Total number of requests made to the snoop filter.

system.membus.snoop\_filter.hit\_single\_requests 82 # Number of requests hitting in the snoop filter with a single holder of the requested data.

system.membus.snoop\_filter.hit\_multi\_requests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data.

system.membus.snoop\_filter.tot\_snoops 0 # Total number of snoops made to the snoop filter.

system.membus.snoop\_filter.hit\_single\_snoops 0 # Number of snoops hitting in the snoop filter with a single holder of the requested data.

system.membus.snoop\_filter.hit\_multi\_snoops 0 # Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data.

system.membus.pwrStateResidencyTicks::UNDEFINED 33361500 # Cumulative time (in ticks) in various power states

system.membus.trans\_dist::ReadResp 474 # Transaction distribution

system.membus.trans\_dist::WritebackClean 80 # Transaction distribution

system.membus.trans\_dist::ReadExReq 75 # Transaction distribution

system.membus.trans\_dist::ReadExResp 75 # Transaction distribution

system.membus.trans\_dist::ReadCleanReq 404 # Transaction distribution

system.membus.trans\_dist::ReadSharedReq 70 # Transaction distribution

system.membus.pkt\_count\_system.cpu.icache.mem\_side::system.mem\_ctrls.port 888 # Packet count per connected master and slave (bytes)

system.membus.pkt\_count\_system.cpu.dcache.mem\_side::system.mem\_ctrls.port 290 # Packet count per connected master and slave (bytes)

system.membus.pkt\_count::total 1178 # Packet count per connected master and slave (bytes)

system.membus.pkt\_size\_system.cpu.icache.mem\_side::system.mem\_ctrls.port 30976 # Cumulative packet size per connected master and slave (bytes)

system.membus.pkt\_size\_system.cpu.dcache.mem\_side::system.mem\_ctrls.port 9280 # Cumulative packet size per connected master and slave (bytes)

system.membus.pkt\_size::total 40256 # Cumulative packet size per connected master and slave (bytes)

system.membus.snoops 0 # Total snoops (count)

system.membus.snoopTraffic 0 # Total snoop traffic (bytes)

system.membus.snoop\_fanout::samples 549 # Request fanout histogram

system.membus.snoop\_fanout::mean 0.003643 # Request fanout histogram

system.membus.snoop\_fanout::stdev 0.060302 # Request fanout histogram

system.membus.snoop\_fanout::underflows 0 0.00% 0.00% # Request fanout histogram

system.membus.snoop\_fanout::0 547 99.64% 99.64% # Request fanout histogram

system.membus.snoop\_fanout::1 2 0.36% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::2 0 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::overflows 0 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::min\_value 0 # Request fanout histogram

system.membus.snoop\_fanout::max\_value 1 # Request fanout histogram

system.membus.snoop\_fanout::total 549 # Request fanout histogram

system.membus.reqLayer0.occupancy 1046500 # Layer occupancy (ticks)

system.membus.reqLayer0.utilization 3.1 # Layer utilization (%)

system.membus.respLayer1.occupancy 2143500 # Layer occupancy (ticks)

system.membus.respLayer1.utilization 6.4 # Layer utilization (%)

system.membus.respLayer2.occupancy 783500 # Layer occupancy (ticks)

system.membus.respLayer2.utilization 2.3 # Layer utilization (%)

---------- End Simulation Statistics ----------